AMENDMENTS TO THE CLAIMS

Claim 1 (Previously Presented): A semiconductor device for comparing an input address with a stored repair address, comprising:

a signal controller for generating control signals and an enable signal;

an address latch unit in response to the control signals for latching the input address;

N number of M-bit address comparators, each for comparing the latched input address with the stored repair address in response to a fuse reset signal and the enable signal;

a comparator modeling block for modeling a replica time for a predetermined time corresponding to address comparing times of the address comparators to delay the enable signal for the replica time; and

a repair circuit controller in response to the delayed enable signal output from the comparator modeling block for generating one of a repair address enable signal and a normal address enable signal based on a comparison result of the address comparators.

Claim 2 (Previously Presented): The semiconductor device as recited in claim 1, further comprising a comparator initialization unit for generating the fuse reset signal to enable and initialize the N number of M-bit address comparators.

Claim 3 (Previously Presented): The semiconductor device as recited in claim 2, wherein each of the M-bit address comparators includes:

a fuse enabling means for receiving the fuse reset signal and the enable signal to thereby output a fuse enable signal in response to whether an enabling fuse included in the fuse enabling means is blown out or not;

a plurality of unit repair address comparing means for respectively comparing each bit of the latched input address with each bit of the stored repair address which is stored in the repair address comparing means; and

a signal combination means for outputting a repair signal in response to results of the plurality of unit repair address comparing means,

wherein the signal combination means is enabled by the fuse enabling signal.

Claim 4 (Original): The semiconductor device as recited in claim 3, the fuse enabling means includes:

a first MOS transistor connected to a supply voltage, gates of the first MOS transistor being supplied with a fuse reset signal;

a second MOS transistor connected to a ground voltage, gates of the second MOS transistor being supplied with the fuse reset signal;

an enabling fuse coupled between the first and second MOS transistors;

a first inverter for receiving a signal supplied between the enable fuse and the second MOS transistor;

a third MOS transistor connected between an input terminal of the first inverter and the ground voltage, gate of the third MOS transistor being coupled to an output terminal of the first inverter;

a second inverter for receiving an output signal from the first inverter;

a first transmission gate for outputting the enabling signal as the fuse enabling signal by turning on when the enable fuse is blown out; and

a second transmission gate for outputting the supplied signal between the enable fuse and the second MOS transistor as the fuse enabling signal by turning on when the enable fuse is not blown out,

wherein the first and the second transmission gates are controlled by output signals from the first and the second inverters.

Claim 5 (Original): The semiconductor device as recited in claim 4, the fuse enabling means further includes a delay means for delaying the enabling signal for a predetermined time.

Claim 6 (Original): The semiconductor device as recited in claim 5, the unit repair address comparing means includes:

a fourth MOS transistor connected to a supply voltage, gates of the fourth MOS transistor being supplied with a fuse reset signal;

a fifth MOS transistor connected to a ground voltage, gates of the fifth MOS transistor being supplied with the fuse reset signal;

an address fuse coupled between the fourth and fifth MOS transistors;

a third inverter for receiving a signal supplied between the address fuse and the fifth MOS transistor;

a sixth MOS transistor connected between an input terminal of the third inverter and the ground voltage, gate of the sixth MOS transistor being coupled to an output terminal of the third inverter;

a fourth inverter for receiving an output signal from the first inverter;

a third transition gate for outputting one bit of the input address to the signal combination means as a comparison signal by turning on if the address fuse is blown out; and

a fourth transition gate for outputting one bit of the inverse input address to the signal combination means as a comparison signal by turning on if the address fuse is not blown out.

Claim 7 (Original): The semiconductor device as recited in claim 6, the signal combination means includes:

a plurality of first NOR gates for receiving the fuse enabling signal and the comparison signal output from the plurality of unit repair address comparing means;

a plurality of first NAND gates for receiving output signals from the plurality of first NOR gates;

a second NOR gate for receiving output signals from the plurality of first NAND gates; and

a fifth inverter for receiving an output signal from the second NOR gate and outputting the repair signal.

Claim 8 (Original): The semiconductor device as recited in claim 7, further comprising a repair address comparison replica which includes:

a third NOR gate for delaying the enabling signal by a delay time of the comparison signal output from the plurality of unit repair address comparing means by a delaying value of the plurality of first NOR gate;

a second NAND gate for delaying an output signal from the third NOR gate by a delay time of the plurality of first NOR gate; and

a fourth NOR gate for delaying an output signal from the second NAND gate by a delay time of the second NOR gate.

Claim 9 (Original): The semiconductor device as recited in claim 8, the repair address comparison replica further includes an output controller for adjusting phase and level of an output signal from the fourth NOR gate in order to equalize phase and level of an output signal from the fourth NOR gate with phase and level of the repair signal which is delivered from the repair address comparing means to the repair circuit controller.

Claim 10 (Original): The semiconductor device as recited in claim 3, the fuse enabling means includes:

a first MOS transistor connected to a supply voltage, gates of the first MOS transistor being supplied with a fuse reset signal;

a second MOS transistor connected to a ground voltage, gates of the second MOS transistor being supplied with the fuse reset signal;

an enabling fuse coupled between the first and second MOS transistors;

a first inverter for receiving a signal supplied between the enabling fuse and the second MOS transistor;

a third MOS transistor connected between an input terminal of the first inverter and the ground voltage, gate of the third MOS transistor being coupled to an output terminal of the first inverter; and

a first NAND gate for receiving the enabling signal and an output signal from the first inverter and outputting the fuse enabling signal.

Claim 11 (Original): The semiconductor device as recited in claim 10, the signal combination means includes:

a plurality of first NOR gates for receiving the fuse enabling signal and the comparison signal output from the plurality of unit repair address comparing means;

a plurality of second NAND gates for receiving output signals from the plurality of first NOR gates;

a second NOR gate for receiving output signals from the plurality of second NAND gates; and

a second inverter for receiving an output signal from the second NOR gate and outputting the repair signal.

Claim 12 (Original): The semiconductor device as recited in claim 11, the repair address comparison replica includes:

a third inverter for receiving the enabling signal;

a third NOR gate for delaying the comparison signal output from the plurality of unit repair address comparing means by a delay value of the plurality of first NOR gates;

a second NAND gate for delaying an output signal from the third NOR gate by a delay value of the plurality of first NOR gates; and

a fourth NOR gate for delaying an output signal from the second NAND gate by a delay value of the second NOR gate.

Claim 13 (Original): The semiconductor device as recited in claim 12, the repair address comparison replica further includes an output controller for adjusting phase and level of an output signal from the fourth NOR gate in order to equalize phase and level of an output signal from the fourth NOR gate with phase and level of the repair signal which is delivered from the repair address comparing means to the repair circuit controller.

Claim 14 (Original): The semiconductor device as recited in claim 1, the repair circuit controller includes:

at least one repair signal combination means for receiving the plurality of repair signals which is output from the plurality of repair address comparing means and driving level of a repair sensing node in response to result of combining the plurality of repair signals;

a repair signal path replica for delaying the enabling signal which passes through the repair address comparison replica for a delay value until the repair signal combination means drives the level of the repair sensing node;

a first output means for outputting a redundancy circuit enabling signal which is used for operating the redundancy circuit in response to the level of the repair sensing node; and

a second output means for outputting a normal circuit enabling signal which is used for operating a normal circuit in response to the level of the repair sensing node after it is enabled by the enabling signal which passes through the repair signal path replica.

Claim 15 (Original): The semiconductor device as recited in claim 14, the repair signal combination means includes:

a plurality of first NAND gates for receiving the plurality of repair signals;

a plurality of first NOR gates for receiving output signals from the plurality of first NAND gates; and

at least one second NAND gate for receiving output signals from the plurality of first NOR gates and driving the level of repair sensing node.

Claim 16 (Original): The semiconductor device as recited in claim 15, the repair signal path replica includes:

a third NAND gate for delaying the enabling signal which passes through the repair address comparison replica for a delay value of the first NAND gates;

a second NOR gate for delaying an output signal from the third NAND gate for delay value of the first NOR gate; and

a fourth NAND gate for delaying an output signal from the second NOR gate for a delay value of the second NAND gate.

Claim 17 (Original): The semiconductor device as recited in claim 16, the repair signal path replica further includes an output controller for adjusting phase and level of an output signal from the fourth NAND gate in order to equalize phase and level of the repair sensing node.

Claim 18 (Original): The semiconductor device as recited in claim 17, the second output means includes:

a fifth NOR gate for receiving the level of the repair sensing node and the enabling signal which is output from the repair signal path replica; and

a buffer for buffering an output signal of the fifth NOR gate and outputting the normal circuit enabling signal.

Claim 19 (Previously Presented): A semiconductor device for comparing an input address with a stored repair address, comprising:

a signal controller for generating control signals and an enable signal;

an address latch unit in response to at least one of the control signals for latching the input address;

N number of M-bit address comparators, each for comparing the latched input address with the stored repair address in response to a fuse reset signal and the enable signal;

a comparator modeling block for modeling a replica time for a predetermined time corresponding to address comparing times of the address comparators to delay the enable signal for the replica time;

a repair circuit controller in response to the delayed enable signal output from the comparator modeling block for generating one of a repair address enable signal and a normal address enable signal based on a comparison result of the address comparators; and

a comparator initialization unit for initializing the N number of M-bit address comparators.

Claim 20 (Previously Presented): The semiconductor device as recited in claim 19, wherein the comparator initialization unit generates the fuse reset signal to enable and initialize the N number of M-bit address comparators.

Claim 21 (Currently Amended): A semiconductor device for comparing an input address with a stored repair address, comprising:

a signal controller for generating an enable signal;

a address comparator for comparing the input address with the stored repair address in response to the enable signal;

a modeling block for modeling a replica time for a predetermined time corresponding to address comparing time of the address comparator to delay the enable signal for the replica time; and

a repair circuit controller for generating one of a repair address enable signal for a redundancy circuit and a normal address enable signal for a normal circuit according to the result of the comparison in response to the delayed enable signal output from the comparator modeling block.

Claim 22 (Previously Presented): The semiconductor device as recited in claim 21, wherein the replica time is duplicated as the comparison time that the address comparator performs.

Claim 23 (Previously Presented): The semiconductor device as recited in claim 22, wherein the repair circuit controller includes:

a repair signal combination unit for receiving the result of the comparison to generate a repair signal;

a signal replica unit for delaying the delayed enable signal output for a modeling time corresponding to the generation time of the repair signal; and

a signal output unit configured to enable a redundancy circuit or enable a normal circuit in response to the delayed enable signal from the signal replica unit.

Claim 24 (Currently Amended): A method for operating a semiconductor device configured to comparing an input address with a stored repair address, comprising:

generating an enable signal;

comparing the input address with the stored repair address in response to the enable signal;

modeling a replica time for a predetermined time corresponding to address comparing time of the address comparator;

delaying the enable signal for the replica time; and

generating one of a repair address enable signal for a redundancy circuit and a normal address enable signal for a normal circuit according to the result of the comparison in response to the delayed enable signal output.

Claim 25 (Previously Presented): The method for operating a semiconductor device as recited in claim 24, wherein the replica time are duplicated as the comparison time that the address comparator performs.